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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,785	09/29/2003	Atsushi Date	03500.017602.	7534

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EXAMINER	
HUISMAN, DAVID J	
ART UNIT	PAPER NUMBER
2183	
MAIL DATE	DELIVERY MODE
08/25/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/671,785	DATE, ATSUSHI	
	Examiner	Art Unit	
	DAVID J. HUISMAN	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 June 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 7-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 7-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-4 and 7-9 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Extension of Time and Amendment as received on 6/3/2008.

Specification

3. The amended title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. Applicant should incorporate, into the title, the concept of granting exclusive access to an on-chip memory to one of an on-chip processor and off-chip processor, and suppressing access requests made by the other.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 3, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto, U.S. Patent No. 4,065,809, in view of Yabushita et al., U.S. Patent No. 5,214,775 (herein referred to as Yabushita).

6. Referring to claim 1, Matsumoto has taught a processor system,

a) wherein the processor system is provided with a first processor (Fig.1, component 11), a memory controller (a system with memory inherently has a memory controller to control accesses to the memory), and a connection unit that mutually connects the memory controller and the processor bus (a processor bus is inherently connected to memory via the memory controller so that instructions/data may be obtained for execution).

b) wherein first and second signal lines for inputting first and second enable signals are connected to reset signal lines of the built-in processor and the external bus interface, respectively, and wherein the first enable signal is asserted while the second enable signal is deasserted, so that issuance of a request for using the processor bus from the first processor can be suppressed and the second processor can use the processor bus exclusively. See Fig.1 and the abstract, and note the WAITa and WAITb signals. Also, see column 4, lines 56-63, and column 6, lines 42-48.

c) and wherein the second enable signal is asserted while the first enable signal is deasserted, so that issuance of a request for using the processor bus from the second processor can be suppressed and the first processor can use the processor bus exclusively. See Fig.1 and the abstract, and note the WAITa and WAITb signals. Also, see column 4, lines 56-63, and column 6, lines 42-48.

d) Matsumoto has not explicitly taught that a single semiconductor substrate includes the first processor (i.e., built-in processor), the memory controller, an external bus interface to which the second processor is connected from outside of the single semiconductor substrate, the processor bus connected with the first processor and the external bus interface, and the connection unit.

However, the examiner asserts that any parts may be integrated on a single chip or made separate, as integration and separation of parts are well known and not patentable features. See *In re Larson 144 USPQ 347 (CCPA 1965)* and *Nerwin v. Erlichman 168 USPQ 177 (1969)*. In addition, Yabushita provides a specific teaching of a processor and shared memory (w/ inherent memory controller) on a single chip and a second processor external to the chip which communicates with the shared memory via an external interface. See Fig.1, Fig.10, the abstract, column 2, lines 65-68, and claim 11, of Yabushita. As a result, since integrating and/or separating is a non-patentable feature, and Yabushita has specifically taught an off-chip processor sharing on-chip memory with an on-chip processor, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Matsumoto such that a single semiconductor substrate includes the first processor, the memory controller, an external bus interface to which the second processor is connected from outside of the single semiconductor substrate, the processor bus connected with the first processor and the external bus interface, and the connection unit. Or, in other words, the WAIT signaling logic of Matsumoto could be employed as at least some of the arbitration logic in Yabushita.

7. Referring to claim 3, Matsumoto in view of Yabushita has taught the processor system according to claim 1, wherein the connection unit includes a common bus. See Fig.1, at least components 28, 39, data bus, and address bus, of Matsumoto.

8. Referring to claim 7, Matsumoto in view of Yabushita has taught the processor system according to claim 1, wherein the built-in processor and the external bus interface are connected through a bus common to the connection unit. See Fig.1 of Matsumoto, and recall that when

modified to include the external bus interface, such a common bus would exist in order to share memory accesses on a single bus, as set forth in Matsumoto.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 2, 4, and 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto in view of Yabushita in view of the examiner's taking of Official Notice.

11. Referring to claim 2, Matsumoto in view of Yabushita has taught the processor system according to claim 1. Matsumoto in view of Yabushita has not explicitly taught that the connection unit is a crossbar switch. However, crossbar switches and their advantages are well known and accepted in the art. A crossbar switch is useful because as the traffic between any two devices increases, it does not affect traffic between other devices. In addition, it is much more scalable than a traditional bus. Consequently, to reduce traffic and increase scalability, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Matsumoto in view of Yabushita such that the connection unit is a crossbar switch.

12. Referring to claim 4, Matsumoto in view of Yabushita has taught the processor system according to claim 1. Matsumoto in view of Yabushita has not taught a second built-in processor connected to the connection unit on the semiconductor substrate. However, systems having multiple processors or being scaled to include multiple processors is known in the art and

advantageous because more processors yield more processing power, and throughput. Consequently, in order to increase performance, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Matsumoto in view of Yabushita to include a second built-in processor connected to the connection unit on the semiconductor substrate.

13. Referring to claim 8, Matsumoto in view of Yabushita has taught the processor system according to claim 1. Matsumoto in view of Yabushita has not taught that the built-in processor and the external processor use in common programs stored in a memory controlled by the memory controller. However, it is knows that a single program may be broken up into pieces to be executed by multiple processors, thereby speeding up execution of that single program. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Matsumoto in view of Yabushita such that the built-in processor and the external processor use in common programs stored in a memory controlled by the memory controller.

14. Referring to claim 9, Matsumoto in view of Yabushita has taught the processor system according to claim 1. Matsumoto in view of Yabushita has not taught an image data transfer bus connected with the connection unit, nor has Matsumoto in view of Yabushita taught an image output device interface or an image input device interface connected with the image data transfer bus on the semiconductor substrate. However, image processing is well known in the art, and in order to obtain image processing functionality in the system of Matsumoto in view of Yabushita, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Matsumoto in view of Yabushita to include an image data transfer bus and an image

output device interface or image input device interface so that images may be transferred to and from the processor for or after processing.

Response to Arguments

15. Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID J. HUISMAN whose telephone number is (571)272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/David J. Huisman/
Primary Examiner, Art Unit 2183
August 6, 2008